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WHAT IS CLAIMED IS:

1. A method of generating a bit error rate estimate for a received signal, the method comprising:

using an error correction decoding technique to generate a block of decoded bits from the received signal;

using an error detection technique to determine whether at least one of the decoded bits from the block of decoded bits has an erroneous value;

if none of the decoded bits from the block of decoded bits has an erroneous value, then calculating the bit error rate estimate from the received signal; and

if at least one of the decoded bits from the block of decoded bits has an erroneous value, then setting the bit error rate estimate equal to a value that is based on a previously calculated bit error rate.

2. The method of claim 1, wherein the step of calculating the bit error rate from the received signal comprises:

using the error detection technique to generate error detection information from the block of decoded bits;

processing the block of decoded bits and the error detection information to generate a synthesized block of coded bits, wherein the processing includes using an error correction coding technique that corresponds to the error correction decoding technique;

using a non-error correction decoding technique to generate a block of raw decoded bits from the received signal;

comparing each bit of the synthesized block of coded bits with a corresponding bit of the block of raw decoded bits; and

setting the bit error rate estimate equal to a value that represents how many bits of the synthesized block of coded bits are not equal to the corresponding bits of the block of raw decoded bits.

3. The method of claim 1, wherein the step of setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises:

setting the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate.

4. The method of claim 1, wherein the step of setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises:

setting the bit error rate estimate equal to a value that is predicted from one or more previously calculated bit error rates.

5. The method of claim 1, wherein the error detection technique includes calculating a cyclic redundancy check.

6. The method of claim 1, wherein the error correction decoding technique includes using Viterbi processing.

7. The method of claim 1, wherein the step of using the error correction decoding technique to generate the block of decoded bits from the received signal comprises:

deinterleaving the received signal to generate a deinterleaved received signal; and

using the error correction decoding technique to generate the block of decoded bits from the deinterleaved received signal.

8. The method of claim 1, wherein the step of setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value comprises:

setting the bit error rate estimate equal to a predetermined value that is not based on the previously calculated bit error rate if the block of decoded bits is at

least an *n*th consecutively received block of decoded bits having at least one decoded bit that has an erroneous value, wherein *n* is a number greater than one; and

otherwise setting the bit error rate estimate equal to the value that is based on the previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value.

9. The method of claim 8, wherein the predetermined value is greater than or equal to a reference value used in a power control algorithm.

10. An apparatus for generating a bit error rate estimate for a received signal, the apparatus comprising:

logic that uses an error correction decoding technique to generate a block of decoded bits from the received signal;

logic that uses an error detection technique to determine whether at least one of the decoded bits from the block of decoded bits has an erroneous value;

logic that calculates the bit error rate estimate from the received signal if none of the decoded bits from the block of decoded bits has an erroneous value; and

logic that sets the bit error rate estimate equal to a value that is based on a previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value.

11. The apparatus of claim 10, wherein the logic that calculates the bit error rate from the received signal comprises:

logic that uses the error detection technique to generate error detection information from the block of decoded bits;

processing logic that processes the block of decoded bits and the error detection information to generate a synthesized block of coded bits, wherein the processing logic includes logic that uses an error correction coding technique that corresponds to the error correction decoding technique;

logic that uses a non-error correction decoding technique to generate a block of raw decoded bits from the received signal;

logic that compares each bit of the synthesized block of coded bits with a corresponding bit of the block of raw decoded bits; and

logic that sets the bit error rate estimate equal to a value that represents how many bits of the synthesized block of coded bits are not equal to the corresponding bits of the block of raw decoded bits.

12. The apparatus of claim 10, wherein the logic that sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises:

logic that sets the bit error rate estimate equal to a value that is equal to the previously calculated bit error rate.

13. The apparatus of claim 10, wherein the logic that sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate comprises:

logic that sets the bit error rate estimate equal to a value that is predicted from one or more previously calculated bit error rates.

14. The apparatus of claim 10, wherein the error detection technique includes calculating a cyclic redundancy check.

15. The apparatus of claim 10, wherein the logic that uses the error correction decoding technique includes a Viterbi decoder.

16. The apparatus of claim 10, wherein the logic that uses the error correction decoding technique to generate the block of decoded bits from the received signal comprises:

a deinterleaver that deinterleaves the received signal to generate a deinterleaved received signal; and

logic that uses the error correction decoding technique to generate the block of decoded bits from the deinterleaved received signal.

17. The apparatus of claim 10, wherein the logic that sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value comprises:

logic that:

sets the bit error rate estimate equal to a predetermined value that is not based on the previously calculated bit error rate if the block of decoded bits is at least an *n*th consecutively received block of decoded bits having at least one decoded bit that has an erroneous value, wherein *n* is a number greater than one; and

otherwise sets the bit error rate estimate equal to the value that is based on the previously calculated bit error rate if at least one of the decoded bits from the block of decoded bits has an erroneous value.

18. The apparatus of claim 17, wherein the predetermined value is greater than or equal to a reference value used in a power control algorithm.